Intel® StrongARM* SA-1111 Microprocessor Companion Chip

Specification Update

May 2002

Notice: The SA-1111 may contain design defects or errors known as errata. Characterized errata that may cause the board's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278260-013

Contents

Revision History

Date	Version	Description
05/30/02	013	Updated the description for SYS_CLK and/or BIT_CLK in Documentation Change Item 3, Doze Mode, Section 2.4.2. Added errata Item 2, Setting the WKUP bit in SACR2 has no affect – Section 7.4.1.3: Serial Audio AC-Link Control Register (SACR2) and errata Item 3, An externally supplied bit clock to the Serial Audio Controller should not be stopped – Section 7.3.2.1: AC-Link Serial Data
11/30/01	012	Corrected Documentation Change Item 4, Control Register (SKCR), Section 3.3.1, by swapping the descriptions of the 0 and 1 state. Added Documentation Change Item 6, PS/2 Trackpad and Mouse Interfaces, Section 9 to enhance the introduction and added Documentation Change Item 11, Control Register (PCCR), Section 12.6.2 to modify the register description.
7/27/01	011	All references to A0 steppings, which were engineering samples, have been removed. This includes errata items 1-6, with respect to –010 spec update and *Markings*. Updated specification change 1, “Add nOE Signal and Register Bit nOE_EN in the SKCR Register” (page 13) for the nOE_EN bit location in the SKCR register. This bit location was reported incorrectly in spec update –010. Modified documentation change 1, “Signal Descriptions: Section 1.4” (page 15), by changing the supply values to “(3.3V **or 5.0 V**)” for pins CFVDD<2:0>. Added documentation change 2, “System Reset, Section 2.3” (page 15), which changed references of VCO_On to VCO_Off in text and in Figure 2-2. Added documentation change 3, “Doze Mode, Section 2.4.2” (page 16), which changed references of VCO_On to VCO_Off in text. Added documentation change 4, “Control Register (SKCR), Section 3.3.1” (page 16), which changed the location of the nOE_EN bit location and clarified bit descriptions in Table 3-9. Added documentation change 7, “GPIO Pin List and Description, Section 10.2” (page 17), which updated the total number of GPIO_A pins in Table 10-1 by adding a row.
2/14/00	010	Updated 278242-003, *Intel® StrongARM* SA-1111 Microprocessor Companion Chip Developer’s Manual,* with documentation changes 1–7, and 9–13, from spec update 009 and removed them from this spec update. Also updated -003 with new register formats, the elimination of all TBD’s, and updated the nOE_EN bit location in the SKCR register. Added documentation change 1, “Signal Descriptions: Section 1.4” (page 15), and document change 8, “Application, Section 11.1.2” (page 17), and document change 9, “Interrupt Sources: Section 11.2” (page 17). Updated specification change 1, “Add nOE Signal and Register Bit nOE_EN in the SKCR Register” (page 13) for the nOE_EN bit location in the SKCR register.
6/30/00	009	Added errata for DMA addressing above 1 MByte relative to the base address of SDRAM memory may result in data corruption. Removed all TBD’s in the *Intel® StrongARM* SA-1111 Microprocessor Companion Chip Developer’s Manual* except for input capacitance and absolute maximum voltage ratings.
3/1/00	008	Remove errata for item 1 through 6 in the GDS1111BA version. Add note to SA-1111 DC Operating Conditions. Update SCLK definition in Section 2.4.2 and Section 8.1.1.
10/21/99	007	Update Figure 7-4 MSB-Justified Data Formats (16 bits).
10/13/99	006	Update nOE_EN bit definitions in the SKCR register and classify the nOE update as a Specification Change.

Date	Version	Description
10/5/99	005	Update SACR0 register definitions. Update nOE definitions. Remove cold-test USB errata. Change status for 5 V IO cell leakage errata to Fix. Change status for 2 KV ESD errata to Fix.
09/22/99	004	Add 5 V I/O cell leakage errata, add 2 KV ESD test errata, and add cold-test USB errata.
09/8/99	003	Add enabling DCLK errata, add pin multiplexing of MSCLK, MSDATA, and PWM1 pins in low-power state errata, add external Bitclk for Serial Audio errata, and add Bitclk, Sysclk, and PS/2 clock errata. All previous document changes (except for some of the TBD's) have been removed from the specification update and applied to the SA-1111 Developer's Manual. Change the description for the ID register.
05/28/99	002	Modify the I/O type for the nOE pin. Modify the assignment for pin 131. Add a note to section 3.2.1. Convert TBD's to values for power and ground pins. Update the descriptions for nSDCS, nSDRAS, and SysClk. Change the normal frequency of UCLK48, UCLK12, and PCLK. Change the enabling condition for the Port Resume interrupt.
04/2/99	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® StrongARM* SA-1111 Microprocessor Companion Chip Developer's Manual	278242-003

Nomenclature

Errata are design defects or errors. These may cause the SA-1111's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® StrongARM* SA-1111 Microprocessor Companion Chip (SA-1111). Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update that will be implemented.
Plan fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	B0	#	#			
1	X			11	No Fix	DMA Addressing above 1 MByte relative to the base address of SDRAM memory may result in data corruption
2	X			12	No Fix	Setting the WKUP bit in SACR2 has no affect – Section 7.4.1.3: Serial Audio AC-Link Control Register (SACR2)
3	X			12	No Fix	An externally supplied bit clock to the Serial Audio Controller should not be stopped – Section 7.3.2.1: AC-Link Serial Data

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	B0	#			
1	X		13	Fix	Add nOE Signal and Register Bit nOE_EN in the SKCR Register

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
1				14		None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	278242-003	15	Doc	Signal Descriptions: Section 1.4
2	278242-003	15	Doc	System Reset, Section 2.3
3	278242-003	16	Doc	Doze Mode, Section 2.4.2
4	278242-003	16	Doc	Control Register (SKCR), Section 3.3.1
5	278242-003	17	Doc	I2S and MSB-Justified Serial Audio Formats: Section 7.3.2.2
6	278242-003	17	Doc	PS/2 Trackpad and Mouse Interfaces, Section 9
7	278242-003	17	Doc	GPIO Pin List and Description, Section 10.2
8	278242-003	17	Doc	Application, Section 11.1.2
9	278242-003	17	Doc	Interrupt Sources: Section 11.2
10	278242-003	19	Doc	Interrupt Sources: Section 11.2
11	278242-003	19	Doc	Control Register (PCCR), Section 12.6.2

Identification Information

Markings

GDS1111BA

This document contains errata for the SA-1111. The revision that is affected by this errata can be identified as order number GDS1111BA. The GDS1111BA can be identified by package marking GDS1111BA, which is the production version and B0 stepping, or by reading the value of 690CC211 in the SKID register.

Errata

1. DMA Addressing above 1 MByte relative to the base address of SDRAM memory may result in data corruption

Problem: When the SA-1111 was programmed to do DMA to addresses above 1 MByte (relative to the base address in that bank of SDRAM), data corruption was found on some transfers. The cause was found to be the erroneous issuance of an AUTOPRECHARGE type of command accompanying the READ command. AUTOPRECHARGE is a variation of the basic READ or WRITE cycle, commanded by asserting address signal A10 at CAS (Column Address Strobe) time, along with the rest of the column address. For SDRAMs, A10 becomes one of the command signals, not an address signal. Since the SA-1110 sets up SDRAMs with burst length = 1, the internal (auto) precharge begins soon after the command is issued, often on top of an extended READ or WRITE burst. This may corrupt data being transferred, or data already stored in SDRAM.

The SA-1111 is designed to use only explicit PRECHARGE commands following the completion of a read or write burst, not AUTOPRECHARGE, so the assertion of A10 at CAS time was in error. Examination of the logic shows that a feature intended to enable operation with EDO DRAMs – for which A10 is always an address bit, not a command signal – is not correctly gated off for operation with SDRAMs. Specifically, one high-order address bit is being enabled through to the SDRAM A10 address. If the address bit is a "1", then A10 will present a HIGH (asserted) state to the SDRAM at CAS time, and the SDRAM will interpret that as an AUTOPRECHARGE command.

Implication: Data corruption may exist on some DMA transfers to SDRAM.

Workaround: The high-order address bit enabled through to A10 is variable, depending on the value of DRAC loaded into bits [4:2] of the SMC control register. DRAC is a function of the number of ROW and (internal) BANK address bits used to address the SDRAM. Table 3-8 of the *Intel® StrongARM* SA-1111 Developer's Manual* shows correct DRAC values to use for a variety of SDRAM organizations. (Note that the number of ROW Address bits in the table is actually the sum of Row Address bits and internal Bank Address (BA) bits as they appear in an SDRAM specification. Usually SDRAMs have four internal banks, so there are two Bank Address bits).
Once the number of ROW address bits is known, the programmer must set up DMA so that a specific high-order address bit is never "1", thus preventing the address from "leaking" through and being interpreted as AUTOPRECHARGE command. This should present little or no impediment to normal operation, because only high-order address bits are involved.
The table below shows which address regions need to be avoided for each of six possible ROW address widths.

Sum of Row + Bank Address Bits	StrongARM Address Bit MUX'd to A10	Example memory regions, relative to SDRAM base address, that work correctly[a]
10	A20	00000000 to 000FFFFF, 00200000 to 002FFFFF etc.
11	A23	00000000 to 007FFFFF, 01000000 to 017FFFFF, etc.
12	A24	00000000 to 00FFFFFF, 02000000 to 02FFFFFF, etc.
13	A25	00000000 to 01FFFFFF, 04000000 to 05FFFFFF, etc.
14	A20	00000000 to 000FFFFF, 00200000 to 002FFFFF etc.
15	A20	00000000 to 000FFFFF, 00200000 to 002FFFFF etc.

a. These regions do not assert the StrongARM address bit that cause A10 assertion.

For example, for ROW + BANK address widths = 10, 14, and 15 bits, the table above describes 1 MByte blocks beginning at SDRAM address 0. Even-numbered blocks (A20 = 0) will work properly, odd-numbered blocks (A20 = 1) will show the problem. For ROW + BANK address width = 11 bits, the blocks are 8 MBytes in size, starting at SDRAM address 0. For ROW + BANK address width = 12 bits, the blocks are 16 MBytes in size. For ROW + BANK address width = 13 bits, the blocks are 32 MBytes in size.

Status: Not fixed.

2. Setting the WKUP bit in SACR2 has no affect – Section 7.4.1.3: Serial Audio AC-Link Control Register (SACR2)

Problem: Setting WKUP to one in SACR2 does not result in assertion of the SYNC output signal.

Implication: A Codec uses SYNC (input) as a wakeup event when in a power-down mode. Without assertion of SYNC, the Codec cannot wakeup.

Workaround: Avoid using the Codec in PR4 mode. The Codec can be used in PR3 mode, but wakeup should be accomplished by the Serial Audio Controller sending a register access command to the Codec that results in the Codec clearing its PR3 bit.

Status: No fix.

3. An externally supplied bit clock to the Serial Audio Controller should not be stopped – Section 7.3.2.1: AC-Link Serial Data

Problem: If an externally supplied bit clock (BIT_CLK) is stopped and then restarted, the Serial Audio Controller remains stopped.

Implication: A Codec stops output of BIT_CLK when placed into the PR4 power-down mode. When the Codec wakes up from PR4 and restarts BIT_CLK, the Serial Audio Controller does not resume operation.

Workaround: Avoid stopping the externally supplied BIT_CLK, e.g., avoid using the Codec in PR4 mode -- the Codec can be used in PR3 mode, but wakeup should be accomplished by the Serial Audio Controller sending a register access command to the Codec that results in the Codec clearing its PR3 bit.

Status: No fix.

Specification Changes

1. Add nOE Signal and Register Bit nOE_EN in the SKCR Register

Issue: The nOE signal was added to control transceiver direction. This signal is enabled by bit 13 in the SKCR register. (This bit was erroneously referred to as bit 12 in the specification update 278260-010).

Affected Docs: *Intel® StrongARM* SA-1111 Microprocessor Companion Chip Specification Update 278260-010* and the *Intel® StrongARM* SA-1111 Microprocessor Companion Chip Developer's Manual*, 278242-003.

Status: Fixed.

Specification Clarifications

1. None for this revision of this specification update.

Documentation Changes

1. Signal Descriptions: Section 1.4

Modify the number of RVSS pins in Table 1-2. Also changed the voltage range for VDD_CF.

Table 1-2. Signal Descriptions

Name	Type	Description
Power and Ground		
VSSX	P/G	Ground supply for all I/O pins, including PCMCIA and CF signals. Pins RVSS<**16**:0> are allocated to this supply.
VDD_CF	P/G	Positive supply (3.3V **or 5.0 V**) for Compact Flash (CF) slot. Pins CFVDD<2:0> are allocated for this supply.

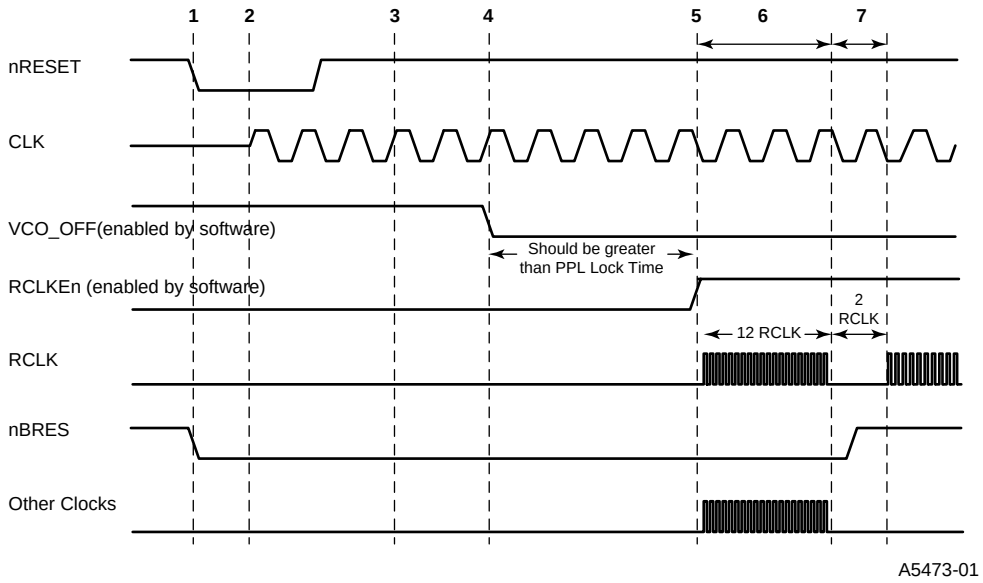
2. System Reset, Section 2.3

Changed VCO_On to VCO_Off in Step 4 of the procedure and clarified the step. Step 4 now appears as follows:

4. VCO_Off is deasserted by software (SKCR Bit <4> =0) and PLL_Bypass is deasserted by software (SKCR Bit <0>=1)

Changed VCO_On to VCO_Off and the signal in Figure 2-2. Figure 2-2 now appears as follows:

Figure 2-2. SA-1111 Reset Sequence



3. Doze Mode, Section 2.4.2

Changed the fourth paragraph to indicate VCO_OFF instead of VCO_ON. The paragraph now appears as follows:

The System Controller and PWM outputs operate independently of the VCO_OFF signal and whether or not the PLL circuit is enabled.

The SYS_CLK and/or BIT_CLK description now appears as follows:

SYS_CLK and/or BIT_CLK
An externally-supplied serial bit-rate clock at 12.288 MHz (from AC'97 Codec device or similar) to the AC-link (or I2S) Serial Audio controller. BIT_CLK can be gated off internally to the SA-1111, putting the AC-link controller into a low-power (off) state.

4. Control Register (SKCR), Section 3.3.1

Changed the location of nOE_EN to bit 13, changed the reset value for VCO_OFF from 0 to 1; enhanced the descriptions for bits 0, and 4; and swapped the enable and disable states for nOE_EN.

Table 3-9. SKCR Bit Descriptions

0x00000000 **SKCR** **SA-1111 Companion Chip**

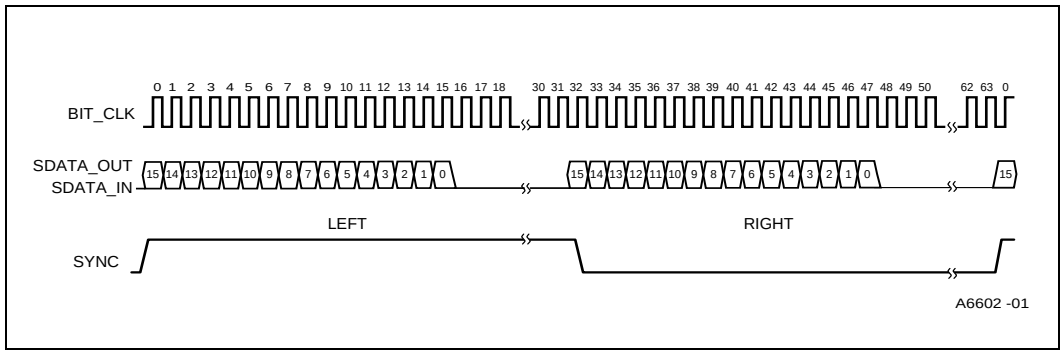
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		nOE_EN	Reserved	UsbIOTestEN	PllTestEn	OPPC	SeLAC	RdyEn	ClockTestEn	ScanTestEn	VCO_OFF	Doze	Sleep	RCLKEn	PLL_Bypass
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bits	Name	Type	Description
0	PLL_Bypass	RW	Specifies on-chip PLL or external source for clocks 1 = Enables the onchip PLL 0 = Bypasses the onchip PLL and uses an external source for clocks.
4	VCO_OFF	RW	VCO (Voltage controlled oscillator) on/off - enables or disables system PLL for clock generation 1= Disables VCO 0 = Enables VCO
13	nOE_EN	RW	Enable nOE assertion on DMA read cycles from SDRAM: 1 = Enable Output Enable 0 = Disable Output Enable (nOE remains high)

5. I²S and MSB-Justified Serial Audio Formats: Section 7.3.2.2

Update Figure 7-4 MSB-Justified Data Formats (16-bits). Figure 7-4 now appears as follows:

Figure 7-4. MSB-Justified Data Formats (16 bits):



6. PS/2 Trackpad and Mouse Interfaces, Section 9

The third sentence in the first paragraph has been changed to indicate that these circuits behave like open-drain circuits. The revised sentence now appears as follows:

The trackpad interface uses the pins TPDATA and TPCLK, and the mouse interface uses the pins MSDATA and MSCLK, all of which behave like open-drain outputs (when in PS/2 mode of operation).

7. GPIO Pin List and Description, Section 10.2

The following row was added in Table 10-1 and now appears as follows:

Table 10-1. GPIO Pin List

GPIO Bit	Function
GPIO_A<4>	USB power control.

8. Application, Section 11.1.2

Modify the description in this section. The description now appears as follows:

The interrupt controller is asynchronous and captures an interrupt without any clocks being enabled. After the interrupt has been captured, however, the internal RAB (Register Access Bus) must be clocked by the 24 MHz RAB clock to read the Interrupt Registers. The RAB clock is controlled by bit 1 in the SKCR register.

When the system is in sleep mode, the wake-up event may be an input to the SA-1111 GPIO. When the wake-up event occurs, it passes through the SA-1111, via the interrupt output to the SA-1110 interrupt (wake-up) input. The SA-1110 performs its wakeup routine and starts the SA-1111 RAB clock to read the Interrupt Registers to determine the source of the interrupt.

9. Interrupt Sources: Section 11.2

Modify the polarity values for interrupts in Table 11-1 (see footnotes a, b, and c).

10. Interrupt Sources: Section 11.2

Table 11-1. Interrupt Sources (Sheet 1 of 2)

Interrupt Number	Name	Source
3:0	GpAInt<3:0>	GPIO_A block inputs (4 total)[a]
9:4	GpBInt<5:0>	GPIO_B block inputs (6 total)[a]
17:10	GpCInt<7:0>	GPIO_C block inputs (8 total)[a]
18	MsTxInt	PS/2 mouse transmit interrupt[b]
19	MsRxInt	PS/2 mouse receive interrupt[b]
20	MsStopErrint	PS/2 mouse stop bit error interrupt[b]
21	TpTxInt	PS/2 trackpad transmit interrupt[b]
22	TpRxInt	PS/2 trackpad receive interrupt[b]
23	TpStopErrint	PS/2 trackpad stop bit error interrupt[b]
24	SspXmtint	Ssp Transmit FIFO empty/under threshold[b]
25	SspRcvint	Ssp Receive FIFO full/over threshold[b]
26	SspROR	Ssp Receive FIFO overrun[b]
27:31	Reserved	—[b]
32	AudXmtDmaDoneA	Audio Transmit DMA Buffer A Done[b]
33	AudRcvDmaDoneA	Audio Receive DMA Buffer A Done[b]
34	AudXmtDmaDoneB	Audio Transmit DMA Buffer B Done[b]
35	AudRcvDmaDoneB	Audio Receive DMA Buffer B Done[b]
36	AudTFSR	Audio Transmit FIFO empty/under threshold[b]
37	AudRFSR	Audio Receive FIFO full/over threshold[b]
38	AudTUR	Audio Transmit FIFO under-run interrupt[b]
39	AudROR	Audio Receive FIFO overrun[b]
40	AudDTS	Audio L3/ACLink Data Sent interrupt[b]
41	AudRDD	Audio L3/ACLink Data Read Done interrupt[b]
42	AudSTO	Audio ACLink read status timeout interrupt[b]
43	USBPwr	USB Controller - power sense input[b]
44	nIrqHciM	USB Controller[b]
45	IrqHciBuffAcc	USB Controller[b]
46	IrqHciRmtWkp	USB Controller[b]
47	nHciMFCir	USB Controller[b]
48	USB port resume	USB Controller[b]
49	S0Readynint	PCMCIA interface[c]
50	S1Readynint	PCMCIA interface[c]
51	S0CDValid	PCMCIA interface[b]
52	S1CDValid	PCMCIA interface[b]

Table 11-1. Interrupt Sources (Sheet 2 of 2)

Interrupt Number	Name	Source
53	S0_Bvd1Stschg	PCMCIA interface[b]
54	S1_Bvd1Stschg	PCMCIA interface[b]
55:63	Reserved	—[b]

a. GPIO interrupts, which are implementation dependant, can have their polarity set to a value of zero (rising) or one (falling).
b. Intel recommends that these interrupts have their polarity set to a value of zero (rising).
c. Intel recommends that these interrupts have their polarity set to a value of one (falling).

11. Control Register (PCCR), Section 12.6.2

Modified the description of bit 7 from S0PSE to S1PSE, and enhanced the bit descriptions for bits 6 and 7.

Table 11-2. PCCR Bit Descriptions

0x0001800 PCCR SA-1111 Companion Chip

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								S1PSE	S0PSE	S1_PWAITEN	S0_PWAITEN	S1_FLT	S0_FLT	S1_RST	S0_RST
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Type	Description
6	S0PSE	RW	Slot 0 PCMCIA Socket Enable If using a 3 V card, set to 0; if using a 5 V card, set to 1.
7	S1PSE	RW	Slot 1 PCMCIA Socket Enable If using a 3 V card, set to 0; if using a 5 V card, set to 1.